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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

7590 10/04/2005

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,293	CHAPEK, DAVID L.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 7/19/05, PROSECUTION IS HEREBY REOPENED. During a thorough review of the prosecution history in this application, is has been determined that the following rejections had not been satisfactorily resolved and thus are being reapplied in this Office action.

To avoid abandonment of the application, applicant must exercise one of the following options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9-12 and 14 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9-12 and 14 include the limitation of the layer of silicon dioxide being free of sputtered metal contaminants. This limitation is indefinite. It is indefinite as to what is required by the limitation "free" of sputtered metal contaminants. Free is a relative term that renders the claims indefinite. Free is a relative term because accepted physics principles dictate that no material will be completely free of metal contaminants, therefore "free" is in fact a relative term. The relative term "free" is indefinite since, in the context of the claims, one of ordinary skill in the art would not know what level of contaminants is required to meet the limitation. The claim does not define any standard for determining the level of contaminants that may be present. Further, the specification does not provide any objective standard for the relative term such that one of ordinary skill in the art would not know what level of contaminants is needed to be considered "free."

4. As best understood, the claims are rejected as follows.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claim 9 is rejected under 35 U.S.C. 102(a) as anticipated by Applicant's admitted prior art.

Applicant's admitted prior art discloses on page 1 lines 12-16 a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon formed on the silicon dioxide, the polycrystalline silicon having a smooth morphology. The admitted prior art discloses the layer of silicon dioxide having been doped with hydrogen ions. Applicants admitted prior art is considered to inherently teach a substrate as the admitted prior art teach DRAM's and DRAM's inherently have a substrate. Though the admitted prior art does not explicitly state a layer of polysilicon is on the silicon dioxide it is implicitly understood that the polysilicon is formed seeing that the admitted prior art discusses performing the hydrogen doping of the silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the silicon dioxide. The admitted prior art does not explicitly state the layer of silicon dioxide being "free of sputtered metal contaminants" but this limitation is considered implicitly understood. In light of the indefiniteness of the relative term "free," the limitation "free of sputtered metal contaminants" is interpreted as meaning sufficiently free so as to operate. Applicant acknowledges in their admitted prior art that even though the device produced using the Kaufman ion source causes some amount of contamination, industry is currently using this method and thus the silicon dioxide layer is "free" of sputtered metal contaminants. Restated, the claim as written is so broad as to read on a conventional layer.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art.

Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, silicon dioxide layer, a layer of polycrystalline silicon over the silicon dioxide layer, and a gate oxide, a source and a drain in the substrate where a gate electrode is formed from the layer of polycrystalline silicon. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16. Applicant's admitted prior art as discussed above also teaches the silicon dioxide as being "free of sputtered metal contaminants." In the combination of the references, the gate oxide would be formed from the layer of silicon dioxide having hydrogen ions implanted therein.

Burns et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon

dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon. The gate oxide for each transistor of the combination of references would be formed of the silicon dioxide having hydrogen atoms implanted therein.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a agte oxide, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Applicant's admitted prior art as discussed above also teaches the silicon dioxide as being "free of sputtered metal contaminants."

Murata et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art to obtain the invention of claim 14.

Response to Arguments

10. Applicant's arguments with respect to claims 9-12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

TOM THOMAS
SUPERVISORY PATENT EXAMINER